

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

2826
BWP

Applicant: Leonard Forbes

Title: SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

Docket No.: 1303.028US1

Serial No.: 09/945,554

Filed: August 30, 2001

Due Date: N/A

Examiner: Thomas L Dickey

Group Art Unit: 2826

Mail Stop Amendment

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

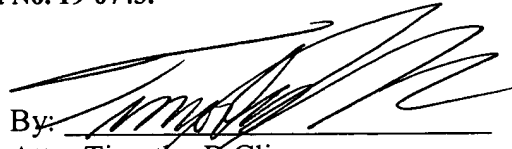
We are transmitting herewith the following attached items (as indicated with an "X"):

- ☒ A return postcard.
- ☒ A Communication Concerning Related Applications (2 pgs.).
- ☒ A Supplemental Information Disclosure Statement (1 pg.), Form 1449 (1 pg.), and copies of 5 cited documents.

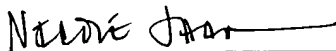
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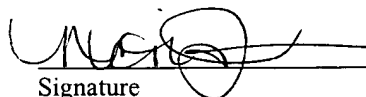
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

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SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.

(GENERAL)

S/N 08/945,554

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes	Examiner: Thomas L. Dickey
Serial No.:	09/945,554	Group Art Unit: 2826
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Title:	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS	

COMMUNICATION CONCERNING RELATED APPLICATIONS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related applications in the above-identified patent application:

<u>Serial/Patent No.</u>	<u>Filing Date</u>	<u>Attorney Docket</u>	<u>Title</u>
10/929,916	August 30, 2004	1303.035US2	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
10/931,704	September 1, 2004	1303.014US2	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/929,986	August 30, 2004	1303.045US2	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW ASYMMETRICAL TUNNEL BARRIER INTERPOLY INSULATORS
10/931,540	August 31, 2004	1303.020US2	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS

COMMUNICATION CONCERNING RELATED APPLICATIONS

Serial Number: 09/945,554

Filing Date: August 30, 2001

Title: SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS

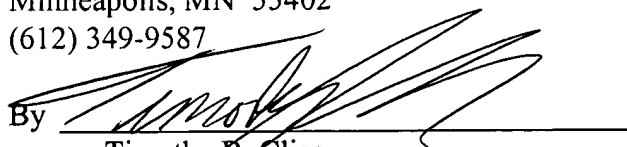
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Respectfully submitted,
LEONARD FORBES

By Applicant's Representatives,
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 349-9587

Date 18 Oct '04

By 
Timothy B. Clise
Reg. No. 40,957

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